CLAIMS

I claim:

1. An apparatus comprising:

a first clock domain to operate at a first clock frequency;

a second clock domain to operate at a second clock frequency; and

an interface disposed between the first and second clock domains to control timing of data transfer from one of the first or second clock domains to other of the first or second clock domains, the interface to allow for a frequency ratio between the first and second clock domains which is not an integer ratio.

2. The apparatus of claim 1, wherein the interface is made programmable to allow selection of different frequency ratios to be selected between the first and second clock domains.

3. The apparatus of claim 1, wherein the interface is to allow for a granularity of 0.25 in the frequency ratio between the first and second clock domains.

4. The apparatus of claim 1, wherein the first clock domain is a bus domain and the second domain is a circuit operably coupled to the bus domain.

5. The apparatus of claim 1, wherein the interface to allow for data transfer in both directions in which first domain operates at a faster frequency than the second domain.

6. The apparatus of claim 1, wherein the interface includes a control circuit to set the frequency ratio and at least one latching circuit to latch data through the interface from one clock domain to the other clock domain.

7. The apparatus of claim 6 further including a plurality of latching circuits, in which separate latching circuits are to be used to transfer data in a particular direction between the first and second clock domains.

8. The apparatus of claim 7, wherein the control circuit of the interface further includes a first and second ratio generators in which the first ratio generator is to be used to generate control signals to the latching circuits, if the ratio difference is below a particular ratio and the second ratio generator is to be used to generate control signals to the latching circuits if the ratio difference is equal to or above the particular ratio.

9. An integrated circuit comprising:

a first clock domain to operate at a first clock frequency;

a second clock domain to operate at a second clock frequency; and

an interface disposed between the first and second clock domains to control timing of data transfer in both directions between the first clock domain and the second clock domain, the interface to allow for a frequency ratio between the first and second clock domains which is not an integer ratio.

10. The integrated circuit of claim 9, wherein the first domain is a bus domain and the second domain is operably coupled to the bus domain to transfer data to and from the bus domain.

11. The integrated circuit of claim 10, wherein the first and second domains are synchronized from a same clock source, but in which the first domain operates at a faster clock frequency than the second domain.

12. The integrated circuit of claim 11, wherein the interface is to allow for a frequency ratio of N:4, where N is an integer, to have a granularity 0.25 for the frequency ratio between the first and second clock domains.

13. The integrated circuit of claim 11, further including a plurality of additional clock domains operably coupled to the bus domain and in which a separate interface is disposed between the bus domain and the additional domains, the interfaces made programmable to allow selection of different frequency ratios to be selected between the bus domain and the additional domains.

14. The integrated circuit of claim 13, wherein individual interfaces include a control circuit to set the frequency ratio and at least one latching circuit to latch data through the interface between the bus domain and respective domain operably coupled to the bus domain.

15. A method comprising:

generating a first clock signal having a first frequency to a first clock domain;

generating a second clock signal having a second clock frequency to a second clock domain, a ratio between the first clock frequency to the second clock frequency being a non-integer ratio; and

using an interface disposed between the first and second clock domains to control timing of data transfer from the first clock domain to the second clock domain, the

interface made programmable to set a particular frequency ratio based on ratio of the first clock frequency to the second clock frequency.

16. The method of claim 15, wherein the first domain is a bus domain and the second domain is operably coupled to the bus domain in transferring data to and from the bus domain, the bus domain operating at a faster clock frequency.

17. The method of claim 16, wherein the ration between the first and second clock frequencies allows for a frequency ratio of N:4, where N is an integer, to have a granularity 0.25 for the frequency ratio between the first and second clock domains.

18. The method of claim 16, further including using a plurality of additional clock domains operably coupled to the bus domain and in which a separate interface is used between the bus domain and the additional domains, the interfaces made programmable to allow selection of different frequency ratios to be selected between the bus domain and the additional domains.

19. The method of claim 16, further including latching data from the bus domain to the second domain by counting a difference in the clock pulses based on the particular frequency ratio and skipping certain ones of excess clock pulses to have a one-to-one data transfer timing between the two clock domains.

20. The method of claim 16, further including latching data from the bus domain to the second domain by counting a difference in the edges based on the particular frequency ratio and skipping certain ones of excess clock edges to have a one-to-one data transfer timing between the two clock domains.